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EXAMINER

PORTKA, GARY J

ART UNIT PAPER NUMBER

2188

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/665,906

Applicant(s)

RAO, G.R. MOHAN

Examiner

Gary J. Portka

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. In view of the appeal brief filed on August 25, 2006, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 8, and 16 recite an array arranged as a single column of predetermined word-width. Applicant has argued that the cited references Mathur and Curtis do not disclose such an array. This argument is derived

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from the argument that the limitation "single column of predetermined word-width" must be read consistent with the interpretation those of skill in the art would reach. The terms "word" and "word-width" (synonymous with "word length") are well defined in the art. According to Microsoft Press Computer Dictionary, word length is the largest amount of data handled by a microprocessor in one operation, or the width of the main data bus, typically 8, 16, or 32 bits. Applicant's meaning for word width includes the particular example of a width of 384 bits. This is clearly beyond the normal meaning of the use of the term (Examiner is not aware of any processor that operates on 384 bits in one operation). Therefore it is contended that one of skill in the art would interpret the term, consistent with the specification, to include any desired length of data transfer size that takes up an entire row of memory. It is a trivial matter that multiple columns may be combined into a fewer number of columns (Applicants own invention may be considered 384 one bit-wide columns combined into a single column). The columns of the references likewise may be considered combined as desired since combining columns in any manner also results in a column. Therefore the argument that the references do not have a single column of predetermined word-width must be based on a position that the memories therein do not have a column of the predetermined word-width, which could only be argued by further positing that the packet of an entire row in the references cannot be considered of a predetermined word-width. Since Applicant contends that 384 bits is a word-width and yet in general a memory row length packet is not, it is not apparent what the term is intended to cover, and therefore it is vague and indefinite. Claims 2-7, 9-15, and 17-21 incorporated these limitations by dependency.

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4. Also, claims 2-4 each recite "said predetermined bit-width", which lacks antecedent basis. Claim 7 recites "the read/write classification", which lacks antecedent basis. Claim 8 recites at line 12 "a said row", which lacks antecedent basis. Claims 9-15 incorporate the limitations of claim 8 by dependency.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2, 7, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Joffe, US 5,440,523.

7. As to claims 1-2 and 16-17, Joffe discloses a *switch/system comprising ports for exchanging data between resources, and shared memory (see Abstract, Figs. 1 and 2, col. 1 lines 13-19) comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width (Figs. 1 and 2, the shared memory having a single column having a word width of k x m bits, see col. 2 lines 7-29), circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port (see*

col. 1 lines 53-64 and col. 2 lines 30-49); *converts from initial bit-width to predetermined width (k to k x m).*

8. As to claim 7, the array of Joffe would have clearly been recognized by an artisan as a random access array of read/write classification.

9. Claims 1-3, 5-8, 10-17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Mathur, US 6,424,658 B1.

10. As to claims 1, 7, 16, and 20, Mathur discloses a *switch/system comprising ports for exchanging data* (see Abstract, Fig. 2), and *shared RAM memory comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width* (Figs. 2 and 3, memory 20 having a single column since a column can be defined as the width of the entry for a single packet, such as packets 3 and 6 in Fig. 9; alternatively, memory 20 has a single column such as col. 1 or cols. 1-2 in Fig. 9), circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port (see Figs. 6 and 7, also in general col. 1 line 55 to col. 2 line 11, col. 4 lines 31-44, col. 5 lines 56-61, which states that column address is not required, supporting the assertion that the memory may be thought of as a single column, also col. 11 lines 44-56).

11. As to claims 2 and 17, Mathur discloses buffers converting the bit-widths (see col. 6 lines 36-65).

12. As to claim 3, in Mathur each packet inherently contains certain bit width and associated overhead.

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13. As to claims 5-6, Mathur discloses available and used address tables (tables 60 and 80 respectively, one each for each port, see Figs. 6 and 7, see col. 9 lines 8-25, and col. 10 lines 1-15).

14. As to claims 8 and 11-15, Mathur discloses the invention substantially as described above with regard to claims 1-7. Mathur additionally discloses a buffer at each port assembling the data stream as recited (see col. 6 lines 36-65). Memory 20 may be considered a plurality of banks (as vertically divided for ports as shown in Fig. 9).

15. As to claim 10, the input port table in Mathur operates as a FIFO as recited.

16. Claims 1-3, 7, 16-17, and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Curtis et al., US 6,925,086 B2.

17. As to claims 1, 7, 16, and 20-21, Curtis discloses a switch/system comprising ports for exchanging data (see Abstract, Fig. 4), and shared memory comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width (see Fig. 1, the memory considered a single column since the segments A-D must all be accessed to access a packet, Fig. 3 and 6, see also col. 1 lines 45-52, and col. 4 lines 19-29), circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port (see Fig. 4, col. 2 lines 38-43, and col. 3 line 63 to col. 4 line 18).

18. As to claims 2 and 17, Curtis discloses buffers converting the bit-widths (since as in Fig. 1 the memory has N 32 bit cells, and the data bus output is 32 bits).

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19. As to claim 3, in Curtis each packet contains certain bit width and associated overhead (Fig. 3).

***Claim Rejections - 35 USC § 103***

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joffe, US 5,440,523.

22. As to claim 3, the embodiment of Joffe cited with regard to claims 1-2 hereinabove (Figs. 1 and 2) does not disclose the bit width includes data and associated overhead. However, another embodiment (Fig. 3) discloses data along with parity (see col. 2 lines 52-57). Parity is one type of overhead associated with data. It would have been desirable to include the parity in the first embodiment, because it is a well known means of preserving data integrity. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to include data and associated overhead, because it was taught by Joffe in a similar embodiment, and one type of which was known to preserve data integrity.

23. As to claim 4, the system of Joffe has the inherent capability of having bit widths of 48 and 384 as recited (by way of the k and the k x m bit widths).

24. Claims 4, 9, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur, or alternatively over Curtis.

25. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur.

26. As to claims 4, 9, neither Mathur nor Curtis disclose initial bit width 48 or predetermined bit width of 384. As to claims 18-19, neither Mathur nor Curtis disclose ATM format. As to claim 21, Mathur does not disclose the recited data interfaces. Each of these limitations were obvious and well known at the time of the invention. The specific bit widths recited fall within the envisioned embodiments of a clearly scalable bit size. Advantages of using ATM format were notoriously well known. Interfaces such as DDR were widely known to have performance benefits. Strobing on both clock edges is akin to DDR and was known to improve performance. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add any of these elements, because they and their advantages were widely known at the time.

### ***Response to Arguments***

27. Applicant's arguments filed in the brief of August 25, 2006 have been fully considered but they are not persuasive.

28. Applicants have argued that Examiner must provide evidence that columns 1-48 of Mathur may be interpreted as a single column of predetermined word-width. Since a column is simply a series of elements arranged vertically, it is trivial that a plurality of columns may be considered a single column; it is also contended that, consistent with the specification, the transfer of a packet to an entire memory row in Mathur may be seen as a predetermined word-width (also see 35 USC 112 rejection hereinabove). Applicants have argued that Mathur does not teach circuitry for writing as recited; Examiner disagrees since all word widths as interpreted above are written and read,

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clearly at different time periods, as recited. Applicants have argued that Mathur does not teach a buffer associated with each port assembling a data stream as recited; Examiner disagrees, the packet buffers are used to assemble a data stream input into packets and vice versa, and are associated with each port as shown in Fig. 3, as recited. A buffer in each port is associated with the port, or alternatively, the buffer may be considered not a part of the claimed port. Applicants have argued that Mathur does not teach shared memory effecting a transfer from one to another port through corresponding buffers, however, all transfers to and from the switch are made through port buffers using the shared memory. Applicants have argued that Mathur does not teach banks. As previously argued by the Examiner, the banks may be considered to be the vertically portioned sections of Fig. 9, such as PORT A, and PORT C; "bank" in general is simply some section or partition of memory. Applicants have argued that Mathur does not teach the plurality of address tables for writing and reading as recited; Examiner disagrees as more fully described hereinabove. Applicants have argued that Mathur does not teach bit-width and overhead, but Examiner maintains that it is well known that the packets as described therein contain data plus overhead. Applicants have argued that Mathur does not teach address table operating as FIFO, but at least the counter of Fig. 6 operates by counting to the end of a packet, thus outputting from the table as a queue. Applicants have argued that limitations of claims 11-15 have not been shown; Examiner disagrees since the memory is a DRAM, stores data corresponding to port, and may include any desired number of ports (that is more than the number of banks). Applicants have argued that the limitation of selection from types

of resources has not been shown; Examiner disagrees since Mathur is a network switch, and thus at least for a digital data network.

29. Applicants have argued that Curtis does not disclose memory of a single column of predetermined word width. Examiner disagrees since as mentioned above with regard to Mathur, a word may be considered a packet, which spans the entire row of the memory. Applicants have argued that Curtis does not teach circuitry for writing data from a port to the array and reading from the array to a port, but the cited sections describe packet data from a port being applied to the packet memory and then to another port. Applicants have argued that Curtis does not teach a buffer associated with each port converting bit width. Examiner disagrees since the memory stores N 32 bit sections and the output port transfer 32 bits at a time; there must be a buffer to transfer between a width and a multiple of the width. Applicants have argued that Curtis does not teach bit-width and overhead, but Examiner maintains that it is well known that the packets as described therein contain data plus overhead. Applicants have argued that the limitation of selection from types of resources has not been shown; Examiner disagrees since Curtis is a packet memory system, and thus at least for a digital data network.

30. Applicants have argued that Examiner has not provided the motivation required to modify the references as stated in the 35 USC 103 rejection; Examiner disagrees since the limitations in question were either within known scaleable variations (changing bit widths), or widely known and providing performance benefits as stated (ATM, DDR, strobing).

**Conclusion**

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 16, 2006

Gary J Portka  
Primary Examiner  
Art Unit 2188

**GARY PORTKA**  
**PRIMARY EXAMINER**



HYUNGSOUGH  
SUPERVISORY PATENT EXAMINER